Liquid Crystal Monitors OEM - Custom

INDUSTRIAL CONSUMER

TECHNICAL INFORMATION

2000

edited by: KEITH PETRI

Flat-panel display

Flat-panel displays offer the small size, light weight, resonably low power consumption. But,
one of the most noticeable and most desirable advantages of LCD, flat-panel monitors over conventional CRT is that they save significant space in any environment.

The next pages will show the technology behind LCD, characteristics, specifications and of course some troubleshooting procedures.

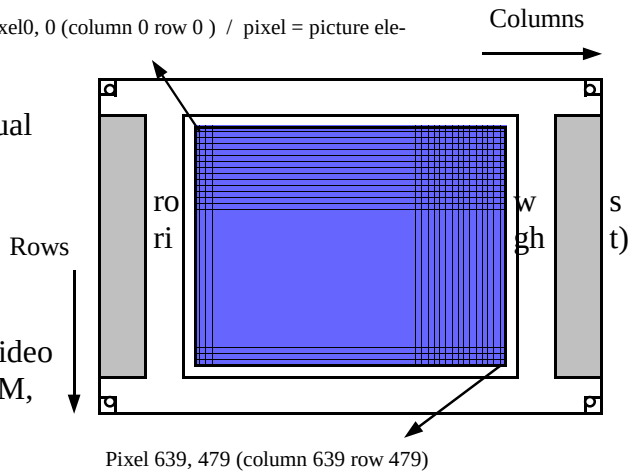
Flat-panel display characteristics

Before entry into a detalied presentation of flat-panel display technologies, it will be helpful to have a clear understanding of a display's major characteristics even if you are familiar already, take a moment to review their handling precautions.

Pixel organization

Images are formed as an array of individual picture elements (*pixels*).
Pixels are arranged into a matrix of (top to bottom) and columns (left to as illustraded in the right fig.

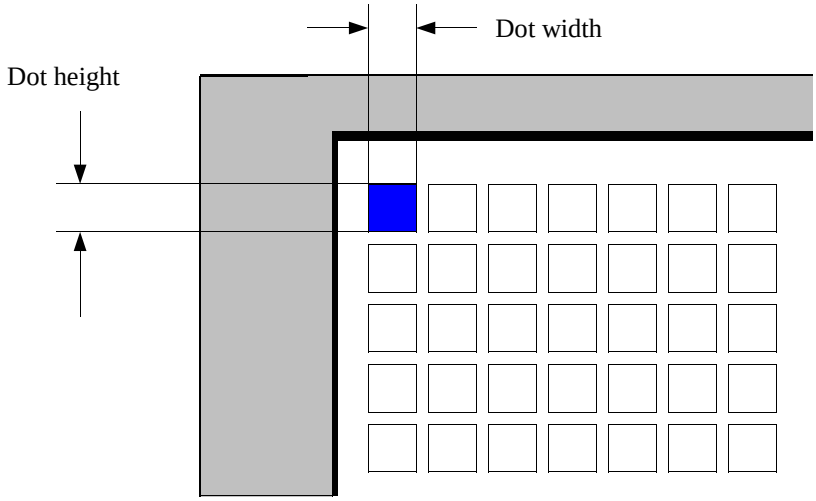
Each pixel corresponds to a location in video RAM. As data are written into video RAM, pixels in the array will turn on and off.



The resolution of a flat-panel display is little more than the number of pixels that can be displayed. More pixels allow the display to present finer, higher quality images.
As an example many lcd's are capable of showing 307,200 dots aranged in a standard VGA array of 640 columns by 480 rows.
The newst systems employ displays capable of handling 480 pixels in an 800x600 format, super VGA or, 1024x768, XGA. As time goes on, flat-panel displays will approach the high resolutions available in current monitors.

Aspect ratio

The aspect ratio is basically the "squareness" of each pixels and indirectly, the squareness of the display. For example, a display with perfectly square pixels has an aspect ratio of 1:1.
A rectangle box 100 pixels wide and 100 pixels high would appear as an even square. Typical
pixels are somewhat higher than they are wide. Higher resolution displays use smaller dots to fit more pixels into roughly the same viewing area. As a result, smaller pixels tend to approach 1:1 aspect ratio. The figure illustrate the concept of aspect ratio.



$$\textit{Aspect ratio} = \frac{\textit{Dot width}}{\textit{Dot height}}$$

Contrast

The *contrast* of an image is loosely defined as the difference in luminous intensity between pixels that are fully on and pixels that are fully off. The greater this diference is, the higher the contrast is, and the image appears sharper. Many flat-panel LCD's offer contrast ranging from a low of 4 to 9 and higher.
The contrast is a comparison of black versus white. It is desirable to simulate 16, 32, 64, or more gray levels that are somewhere between black and white. Do not confuse gray scale with poor contrast.

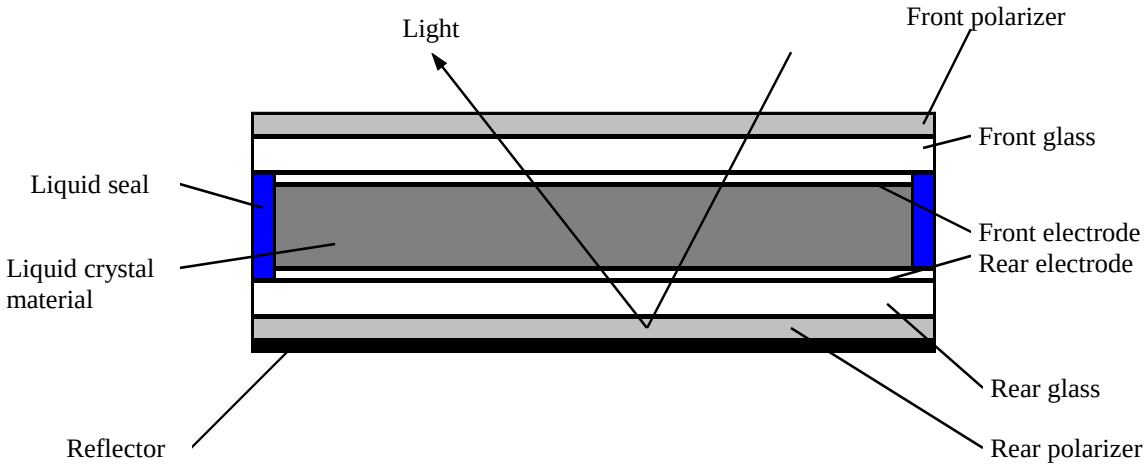
Handling precautions

Next to magnetic hard drives, flat-panel displays are some of the most sophisticated and delicate assemblies in the computer industry. You must be extremly careful with **all** liquid crystal (LC) assemblies. Liquid crystal material is sandwiched between two layers of fragile glass. The glass can easily be fractured by abuse or careless handling. If a fracture should occur and liquid crystal material happens to leak out, use rubber gloves and wipe up the spill with soap and water.
You can use very gentle pressure to clean the face of a display. Lightly wet a soft, clean cloth with fresh isopropyl alchool, then gently wipe away the stain. Never use water or harsh solvents to clean a display. Liquid crystal material coagulates (become firm) at low temperature (below 0 degree C).

LCD technology

LC exhibits a crystalline molecular structure that resembles a solid. In its normal state, LC is virtually clear; light would pass right through a container of LC. When LC material is assembled into a flat panel, the molecules have a tendency to twist. It was discovered that a voltage applied across a volume of LC forces the molecules between the active electrodes to straighten. When the voltage is removed, the straightened LC molecules return to their

normal twisted orientation. Futher words will revealead an interesting phenomenon when light polarising materials (or polarizers) are placed on both sides of the LC layer; areas of the LC material that are excited by an external voltage become dark and visible. When voltage is removed, the area becomes clear and invisible again. A polarizer is a thin film which allows light to pass in only one orientation.By using electrodes with different patterns, various images can be formed. A **typical LCD** assembly is illustrated bellow. An array of transparent electrodes are printed and sealed on the inside of each glass layer.

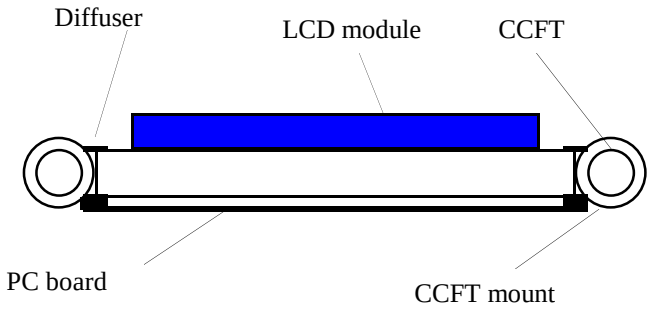


A conventional LCD display

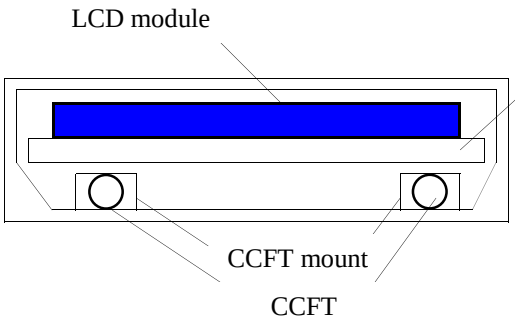
It is important to realize that light plays a critical role in the formation of liquid crystal images
The path that the light takes through the LC assembly and your eyes can have a serious impact on the display's image quality as well as the display's utility in various environments.

Backlighting

There are few primary approaches to backlighting:
electroluminiscent (EL) panels, cold-chatode fluorescent tubes (CCFTs), light emitting diodes
(LEDs).
Due to some inconveniences, (short working life...) we do not describe EL panels and LED's (LED are not yet available in white light configurations that are favored for computer applications).
Cold-cathode fluorescent tubes (CCFTs) offer a very bright source of white light that consumes reasonable little power. they also enjoy a long life (20,000 to 50,000 h) without serious
degradation. Such characteristics have made CCFTs very popular in a great notebook display applications. Custom OEM designs are available for any light output specified. This is accomplished by adding or substracting CCFT's from the design as necessary.



Edge lighting
(double tube design)



Rear lighting
(double-tube design)

CCFT backlight configurations.

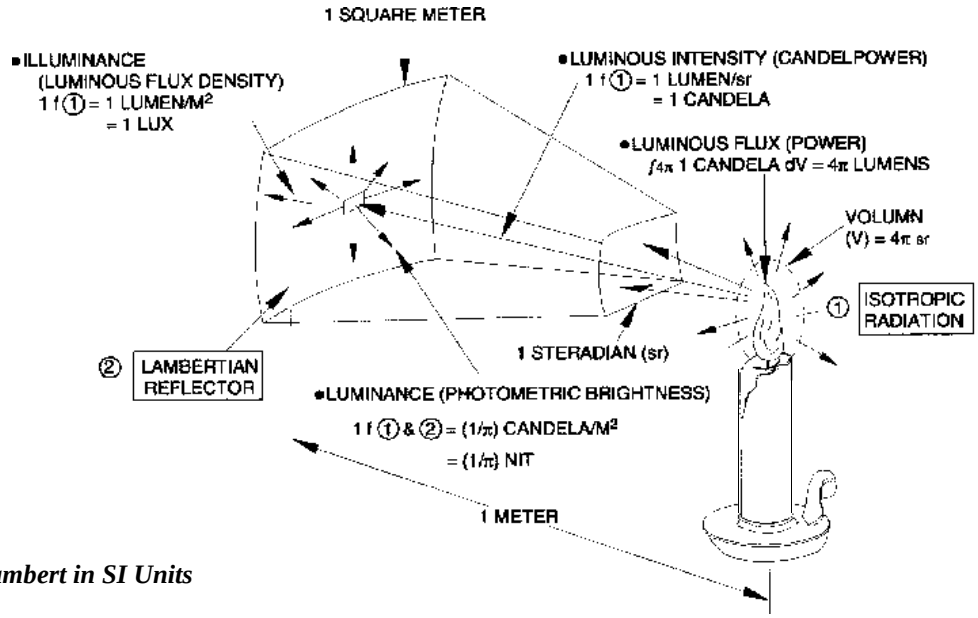
Most lamp technologies require specialized electronic drive methods. Typically, DC to AC inverters are the most common drive method. Special features include: Dimming, on/off and other control functions.

MEASUREMENTS AND DEFINITION

It is well known that many terms used in our every-day technical discussion are often misused, such as brightness vs. luminance and resolution vs. display format. The two primary measurements used in display image quality characteristics are luminance and spectral radiance. Resolution is also important in defining the interaction between the information density on the display and the resolving capability of the human visual system.

LUMINANCE

Luminance can be defined as the quantitative measure of brightness and is measured in English units as footlamberts (fL) and in SI (International System) units as candela/m^2 Another term which is commonly used in North America , is **nit.** The relationship is one nit = 0.2919 footlambert.



Footlambert in SI Units

A footlambert is the luminance reflected off a square foot Lambertian (perfectly diffusing) reflector iluminated by 1 candle (fc). Some electrical equivalent term's are described bellow:

ELECTRICAL	LUMINOSITY TERM	LUMINOSITY UNIT
Power (rate of energy flow)	Luminous Flux	Lumen = 1/680 watt/Luminosity
Power-source Output	Intensity (Power-Source)	Candela = Lumen / Steradian
Delivered Power	Luminance (Surface)	Nit = Candela / m^2
Power-transfer Efficiency	Transmittance	Transmittanc Factor = 0.0 to 1.0
	Reflectance	Reflectance factor = 0.0 to 1.0

COLOR

One of the best way to describe the three dimentional color characteristics (luminance, hue and saturation in a two dimentional chart is by using the CIE System (Commission Internationale de L'Eclairage). Any color can be characterized by its x and y coordinates. The chart assumes all colors are generated by equal radiance sources, which puts white at the center of the chart. Color temperature is often used to specify white balance.

CONTRAST RATIO

All ambient and display parameters must be defined in order to calculate contrast ratio.

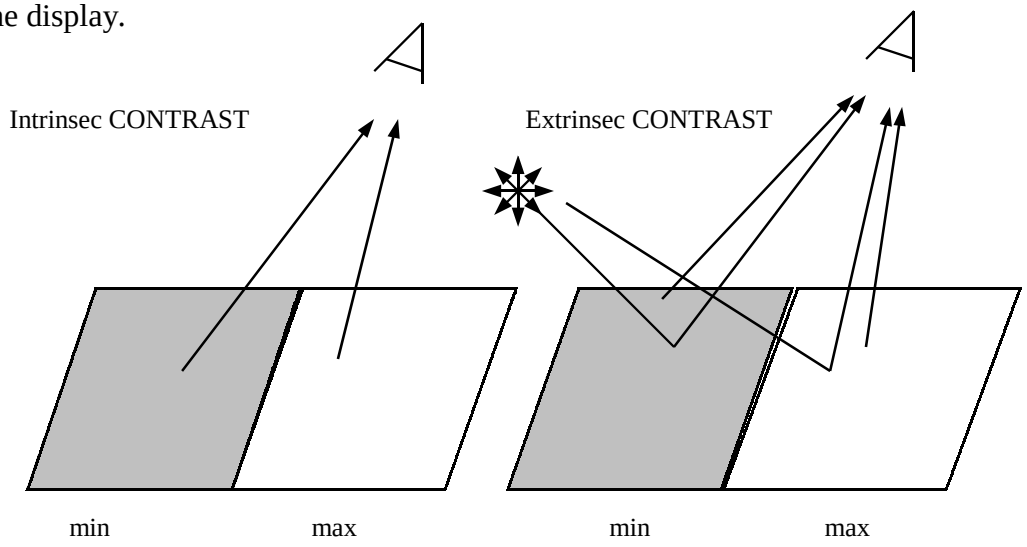
$$\text{Contrast ratio} = \frac{\text{Maximum Luminance}}{\text{Minimum Luminance}}$$

In LCDs the angle of measurement to the display surface should be defined as the contrast ratio varies over the angle. As long as all conditions are controlled and noted, an accurate comparison of displays can be made.

VIEWING ANGLE

Because there are limitations inherent to the technology, the viewing angle defined as

contrast ratio over a certain angle. This angle is specified by its x and y direction on the face of the display.



CONTRAST RATIO

RESPONSE TIME

Response time is the time it takes a pixel to change state from on to off ("black" to "white"). This time includes all electrical and physical delays. It is defined as the transition time from the 10% level to the 90% level of luminance output. Rise and decay times may be combined to give a total response time.

CONCLUSIONS

As has been explained, image quality is characterized by a close interaction between the display and human eye. Unfortunately, sometimes in the end, it may be a subjective visual response that determines the choice of the display, contrary to measured data.
With the understanding of the terminology used in image quality analysis, it is intended to keep subjective decisions to a minimum.

1999 - More than a Few Products

At the end of 1998, KRISTEL started in paralel with production of CRT's displays, the "flat panel display" production. At this time we are able to offer a new family of enclosed Liquid Crystal Monitors.
Even with our wide product selection, we realize that customer requirements may demand a special product. Accordingly, we can develop custom design solution through the talents of our Design Engineering, Applications Engineering and Mechanical Design department. They are backed by our dedication to providing long-term product availability for our OEM design .

Quality Products

When you buy a product from KRISTEL, you're buying much more than a package of parts. In addition to the assistance from your Kristel Applications Engineer and the Design engineering, you are also purchasing the quality assurance that is central to each step in our manufacturing process. This process is geared toward a specific goal: production of consistent, quality products that will perform properly in a wide range of operating environments.
Our 65,000 sq. ft. manufacturing plant common with CRT display production is specially designed for a production flow for both CRT and LCD. Some highlights of our quality assurance operations are described bellow:
Surface mount of our entire spectrum PCB's is done in our plant in Taipei / Taiwan. We have our own surface mount line to assure control over this critical phase of production. On fine pitch parts, solder quality is inspected under 20 x magnification to ensure performance. This step is especially important to guarantee the quality of connections for proper operation in high-vibration environments.
Prior to use in any application, each board begins its extensive electrical test . This test verifies the function of each circuit and previous step in the production process
When everything is right, the pcb's is assembled in our LCD display, and sent for final test and inspection.

System Assembly Documentation

Kristel flat panel displays are built to customer order in our systems assembly area. Extensive
documentation produced and maintained by our Manufacturing Engineering department guarantees that our LCD panels display are built consistenly from order to order.
This consistency is especially important to OEMs who integrate Kristel liquid crystal units into their end-products, often over a multi-year period.

Final Quality Control

After a finished flat panel display assembly have been final tested to ensure proper operation, they enter our final QC checkpoint. All units are 100% inspected visually and electrically.
Only if they pass this inspection, are they “Ready To Ship”

Flat facts

Also, Kristel offers a large range of touchscreen integration for our LCD product with good durability and resolution, based on resistive technology, Capacitive or AW (Acoustic Wave).

KRISTEL CORPORATION

KC10.4 (VGA)

- 640 x 480 Pixel TFT Color Display
- 196 x 161.1mm (10.4") Active Area
- 110ms Fast Response Time
- 70cd/m^2 High Surface Brightness
- 20:1 High Contrast Ratio
- Wide Viewing Angle (Horizontal=50^0, Vertical=60^0
- Over 25,000 Hours Long Life CCFT x 1
- No Electromagnetic Radiation
- Low Power Consumtion

KC12S41 (SVGA)

- 800 x 600 Pixel Active Matrix Color Display
- 246 x 184.5mm (12.1") Active Area
- 270cd/m^2 High Surface Brightness
- 300:1 High Contrast Ratio
- Wide Viewing Angle (Horizontal=110^0,Vert.=140^0)
- Over 30,000 Hours Long Life CCFT x 2
- No electromagnetic Radiation
- Ultra Low Power consumtion
- Single Supply Voltage (3.3V)

KC14X03E (XGA)

- 1024 x 768 Pixel Active Matrix Color Display
- 276.6 x 209.7mm (13.8") Active Area
- 200cd/m^2 High Surface Brightness
- 300:1 High Contrast Ratio
- Wide Viewing Angle (Horizontal=110^0, Vertical=140^0)
- Over 20,000 Hours Long Life CCFT x 2
- No Electromagnetic Radiation
- Ultra Low Power Consumtion
- Single Supply Voltage (3.3V)

KC15X01 (XGA)

- 1024 x 768 Pixel Active Matrix Color Display
- 304.1 x 228.1mm (15") Active Area
- 200cd/m^2 High Contrast Ratio
- Wide Viewing Angle (Horizontal=120^0,Vertical=140^0)
- Over 25,000 Hours Long Life CCFT x 2
- No Electromagnetic Radiation
- Ultra Low Power Consumption
- Single Supply Voltage (3.3V)

KRISTEL CORPORATION


KC400S

- 640 x 480 Pixel 10.4" DSTN LCD Monitor
- 256 Colors and 70 cd/m^2 High Brightness
- Over 20,000 Hours Long Life CCFT x 1
- Wide Operation Range (5^0C - 40^0C)
- High Color Digital Interface Display Card Delivers Animated Pictures
- VESA DPMS Power Management
- TTL Level / LVDS Transmit


KC700ST

- 800 x 600 Pixel 12.1" TFT LCD Monitor
- 262K Colors and 270 cd/m^2 High Brightness
- Over 30,000 Hours Long Life CCFT x 2
- Wide Operation Range (0^0C - 50^0C)
- Light Weight (2.0kg) and Space-saving
- High Color Digital Interface Display Card Delivers Animated Pictures
- VESA DPMS Power Management


KC800XTA

- 1024 x 768 Pixel 13.8" TFT LCD Monitor
- 262K Colors and 200cd/m^2 High Brightness
- Over 20,000 Hours Long Life CCFT x 2
- Wide Operation Range (0^0C - 50^0C)
- Analog Interface for Direct Interface to any PC graphics card
- Screen solutions suportted VGA, SVGA and XGA
- TTL level, Positive/Negative Separate Sync
- VESA DPMS Power Management
- External AC / DC Adapter, Power Cord, VGA Cable


KC900XTA

- 1024 x 768 Pixel 15" TFT LCD Monitor
- 262K Colors and 200cd/m^2 High Brightness
- Over 25,000 Hours Long Life CCFT x 2
- Operation Range (5^0C - 45^0C)
- Analog Interface for Direct Interface to any VGA card
- Resolution Supported VGA, SVGA and XGA
- TTL level, Positive / Negative Separate Sync
- VESA DPMS power management
- External AC / DC Adapter, Power Cord, VGA cable

Display system description

The components of an LCD Display are:

- a microprocessor
- a system controller (if used)
- some amount of video memory (VRAM)
- a backlight voltage source
- a highly integrated display controller IC
- a flat panel display assembly itself

The microprocessor is responsible for executing the instructions contained in BIOS.
As the CPU executes its programs, it directs the operations of a system controller IC.
While it is not mandatory that a computer utilize a system controller, a single controller IC can effectively replace dozens of discrete logic ICs.

The display controller IC is addressed by the system controller over the common system address bus. This is the “video adapter” for small computers. Once the display controller is addressed, the system controller writes display information and comands over a secondary data bus. A clock and miscellaneous control signals manage the flow of data into the display controller. Each pixel in the physical display can be traced back to a specific logical location (address) in VRAM. As new data are written to the display controller, VRAM addresse are updated to reflect any new information.
During an update, the display controller reads through the contents of VRAM and sends the data along to the flat-panel display. There are two other signals required by an LCD assembly: contrast voltage and backlight input voltage.

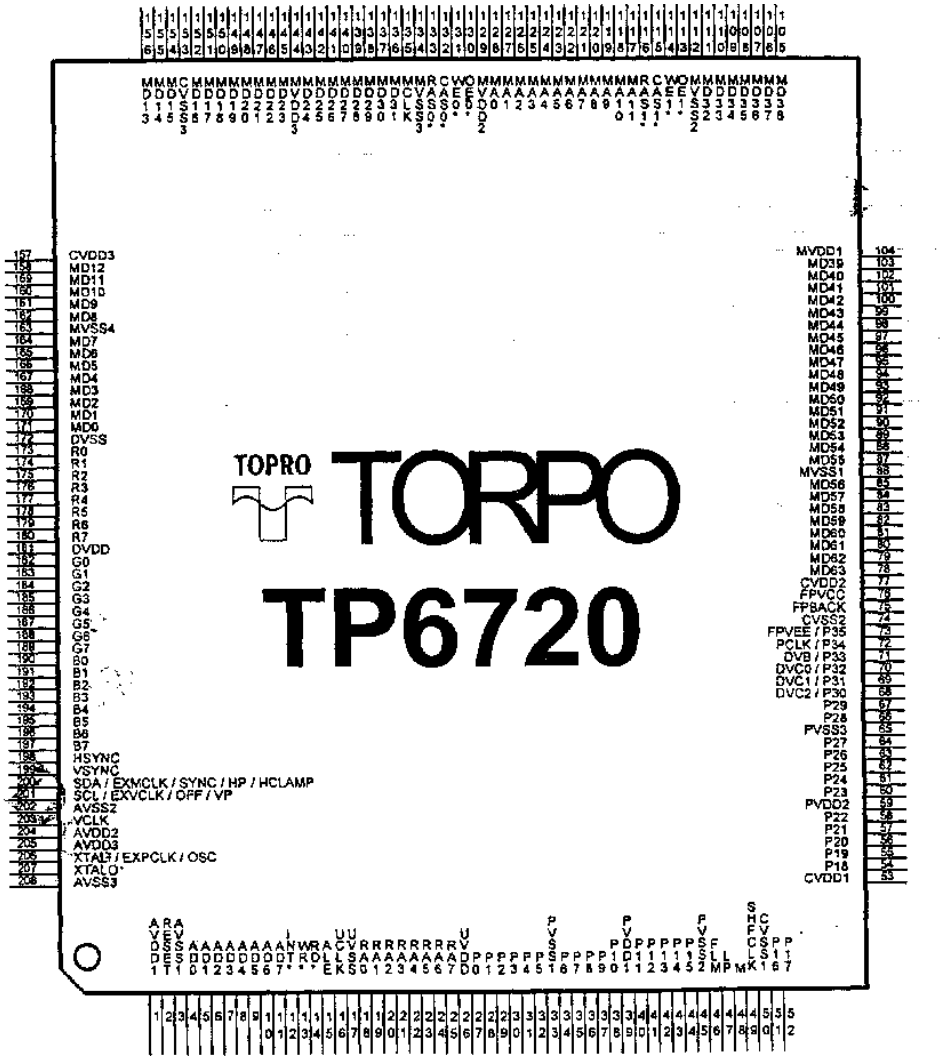
Most Kristel application use Topro technology / 10",12" VGA, SVGA/. The following is a brief description of the TOPRO TP6720Q (APMC)

TP 6720Q

It's a single-chip *analog panel controller*, with easy-to-operate and powerful features, used in flat panel monitor. It contains all the logic required to convert PC VGA signals to color TFT/DSNT LCD signals. TP6720 uses 208 pins , surface mount only.

The TP6720 includes *Memory Controller (MEMC), OSD Controller (OSDC), Display Mode Detector (DMD), Address Multiplexer (AMUX), Power Management Controller (PMC) PLL Frequency Synthesizer, Flat Panel Controller, RGB Space Converter* .
The TP6720 supports best system performance even in minimum memory configurations. The processor includes a builit-in Frame Rate controller to adjust the input horizontal/vertical sync
polarity and to provide the input/output frame rate control. It also implements a VESA DDC interface to communicate with users through VGA card and PC system.
The TP 6720 suports flat panel display with resolution up to 1024x768 true-color. The flat panel interface supports Monochrome, color STN LCD panel, color TFT LCD panel with direct panel interface to (DD) Dual-panel, Dual drive for color and monochrome and (SS)

Pin Configurations



Pin Description

SYMBOL	Pin Number	Function	Type
MPU Bus Interface			
AD [7:0]	11,10,9,8,7,6,5,4	Address and data are multiplexed on the same MPU bus interface. A bus transaction consists of an address phase followed by one or more data phases	I/O
RA [7:0]	25,24,23,22,21,20,19,18	This signals are lached from AD [7:0] bus. They perform as the low address of external ROM of MPU.	OT
RESET	2	The signal is used to reset the TP6720 into initial state.	I/S
ALE	15	used to latch those MPU's otput address	I
INT*	12	This signal is used to latch those MPU's otput address.	O
WR*	13	Indicates a write operation. An active-high input is valid for read cycle	I
RD*	14	Indicates a read operation. An active-high input is invalid for a read cycle	I
UCLK	16	This signal is a clock source for MPU	O
RGB Input Interface			
R[7:0]	180,179,178,177,176,175,174,173	These signals provide digitized 8-bit 3-channel data from external analog-to-digital converter	I
G[7:0]	189,188,187,186,185,184,183,182		I
B[7:0]	197,196,195,194,193,192,191,190		I

SYMBOL	Pin Number	Function	Type
HSYNC	198	Horizontal synchroniza-tion signal comes from VGA connector	I/SL
VSYNC	199	Vertical sync. signal comes from VGA conn.	I/SL
VCLK	203	This signal is output as a sampling	O
Clock Input Interface			
XTALI	206	The pin serves as the crystal input	I
XTALO	207	The pin serves as the crystal output	O
Memory Interface			
MA[11:0]	117,118,119,120,121,122, 123,124,125,126,127,128	Frame buffer address bits are from 11 to 0 for DRAMs. For 256kx16-bit EDO DRAMs,only MA[8:0] are used.	O
MD[15:0] MD[31:16]	136,137,138,139,140,141, 142,143,145,146,147,148, 149,150,151,152,154,155, 156,158,159,160,161,162, 164,165,166,167,168,169, 170,171	These pins are used to transfer data between TP6720 and frame buffer.When memory bus is 64-bit data width, these pins are used to transfer lower 32-bit data.	I/O/U I/O
MD[63:32]	78,79,80,81,82,83,84,85, 87,88,89,90,91,92,93,94, 95,96,97,98,99,100,101, 102,103,105,106,107,108, 109,110,111	Used to transfer upper 32-bit data between the TP6720 and frame buffer for 64-bit data width of memory bus.	I/O
RASI* RASO*	116 133	Row address strobe for latching 12-bit row ad-dress signal into buffer	O O
CAS1	115	Column address strobe signal	O

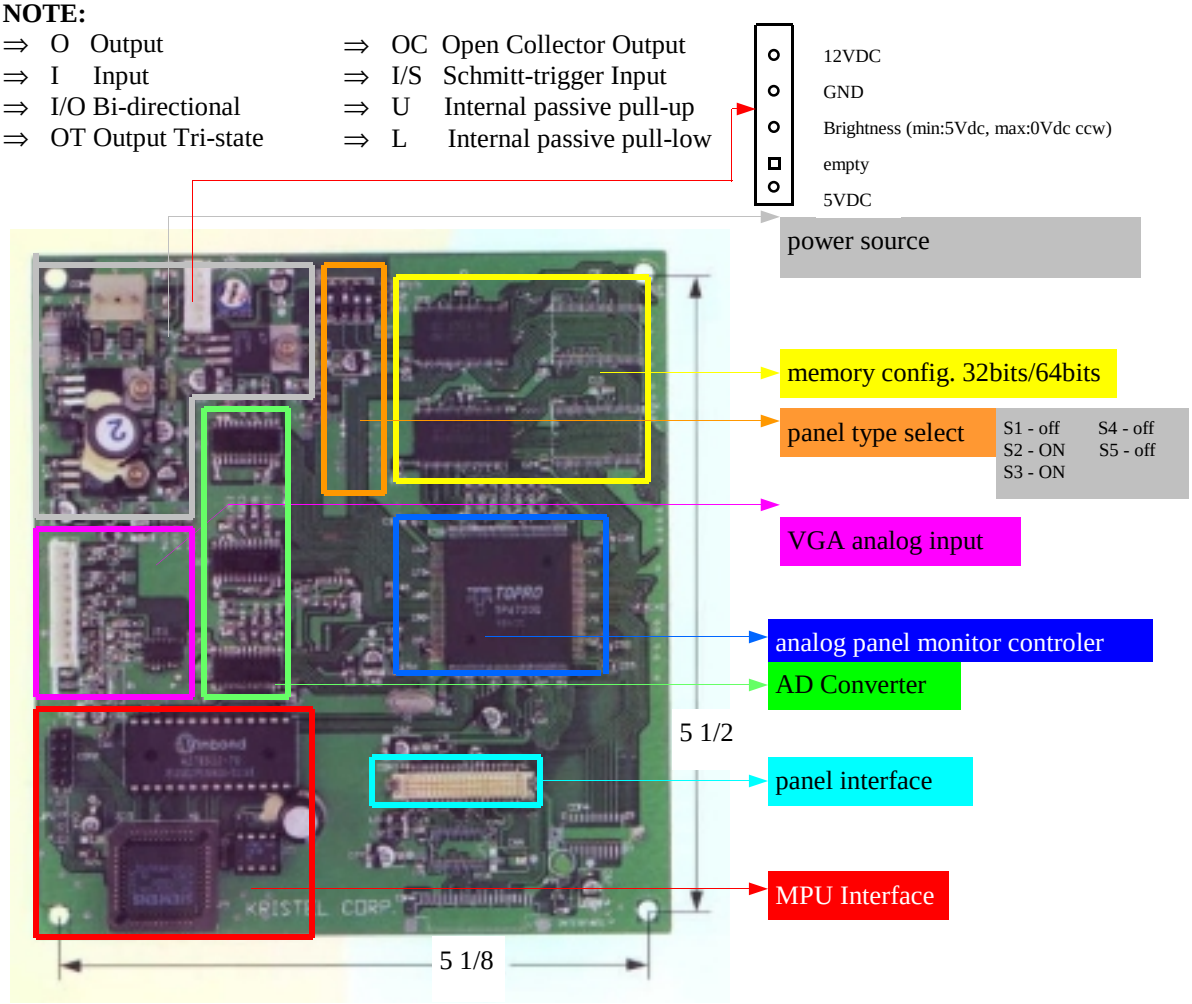
SYMBOL	Pin Number	Function	Type
CAS0*	132	address strobe signal	O
WE1*	114	Write enable signal for DRAMs	O
WEO*	131		O
OE0*	130	Data enable signal for lower 2M-byte DRAMS	O
OE0*	113	Data enable signal for upper 2M-byte DRAMs	O
MCLK	135	Is a clock source for external SDRAMs	O
VESA DDC Interface			
SDA /EXMCLK /SYNC /HCLAMP /HP	200	VESA DDC2 data output It can be redefined as a memory clock input or TV comp. sync. signal output. Horizontal clamp signal Adjusted positive polarity Horiz. synchronization signal output.	I/OC I O O O O
SCL /EXVCLK /OFF	201	VESA DDC2 clock signal It can be redefined as a VGA clock input or power saving input pin	I/O I I
/VCLAMP		Vert.clamp signal output	O
/VP		Adjusted positive polarity vert.synchronization signal output	O
SHFCLK(CL2)	49	This signal is used to drive the flat panel shift clock	O
LP(CL1) / PHSYNC	47	Drive the flat panel line clock for LCD or the Hsync for TFT panels	OT

FLM /PVSYNC	46	This signal is used to start a new frame on flat panels for LCD or the Vert.sync for TFT panels	OT
M /DE	48	is used to provide the AC inversion to prevent chemical damage.	O
P[35:0]	73,72,71,70,69,68,67,66, 64,63,62,61,60,58,57,56, 55,54,52,51,44,43,42,41, 40,38,37,36,35,34,32,31, 30,29,28,27	This signal contain R/G/B color data for 9/12/15/16/18/24/36-bit data interface of flat panels	O
FPVCC	76	signal used for the flat panel power-down seq.	O
FPBACK	75	same as above, should be connected to the flat panel Logic power cable	O
SCL	203	VESA DDC2 clock output	I(I/O)
Power Pins			
AVDD1	1	Internal MCLK frequency Synthesizer power	+5V
AVDD2	204	Internal VCLK frequency Synthesizer power	+5V
AVDD3	205	Internal VCLK frequency Synthesizer power	+5V
CVDD[3:1]	157,77,53	Core logical power	+5V
DVDD	181	Digital pads output power	+5V
MVDD[3:1]	144,129,104	Mem. bus interface power	+5V
PVDD[2:1]	59,39	Flat panel interface power	+5V
UVDD	26	MPU bus interface power	+5V
AVSS1	3	Internal MCLK freq. Synthesizer analog ground	Ground
AVSS2	202	Internal VCLK analog gd.	Ground

AVSS3	181	Internal PCLK freq.Synth.analog gnd	Ground
CVSS[3:1]	153,74,50	Core logical ground	Ground
DVSS	172	Digital pads output gnd.	Ground
MVSS[4:1]	163,134,112,86	Memory bus interface gnd	Ground
PVSS[3:1]	65,45,33	Flat panel interface gnd.	Ground
UVSS	17	MPU bus interface gnd.	Ground

NOTE:

⇒ O Output
⇒ I Input
⇒ I/O Bi-directional
⇒ OT Output Tri-state
⇒ OC Open Collector Output
⇒ I/S Schmitt-trigger Input
⇒ U Internal passive pull-up
⇒ L Internal passive pull-low



LQ12S41 Color TFT-LCD Module

FEATURES

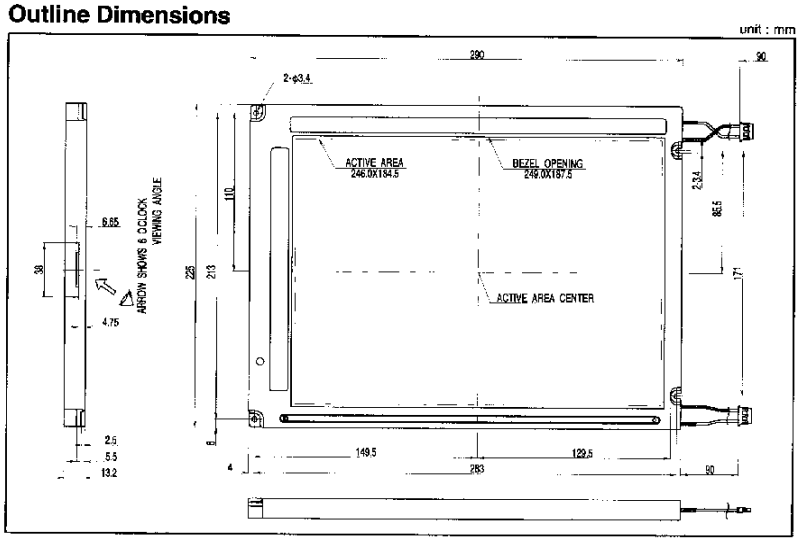
- 31 cm [12.1”] SVGA format
- Built-in long life (30.000 h) backlight
- High Brightness: 250 cd/m^2
- Wide viewing angle: L/R 120

SPECIFICATIONS

Parameter		Unit
Display size	31[12.1]	cm[“]
Dot format HxV	800xRGBx600	dot
Dot pitch (HxV)	0.1025x0.3075	mm
Active area (HxV)	246.0x184.5	mm
Color	262144	-
Input Signal	6-bit Digital RGB	-
Backlight type	2CCFT (E)	-

Parameter		Unit
Brightness	270	cd/m^2
Contrast ratio	300:1	-
Power consump. (& backlight)	7.5	w
Dimensions	290.0x225.0x13	mm
Weight	990	g
Operating temp.	0 to +50	C
Storage temp.	-25 to +60	C

Outline Dimensions



OVERVIEW

The SHARP module is a color active matrix LCD incorporating amorphous silicon Thin Film Transistor (we call "TFT"). It is composed of a color TFT-LCD panel, driver IC's, control circuit, power supply circuit and a backlight unit. Graphics and texts can be displayed on a 800x600 dots panel with 262,144 colors by supplying 18 bit data signal
(6bit /color). Four timing signals, +3.3V/5V DC supply voltage for TFT-LCD panel driving and supply voltage for backlight.
The TFT-LCD panel used for this module is a low-reflection and higher-color-saturation type. Therefore, this module is suitable for all kinds of applications.
This module type is of wide viewing angle and high brightness (250cd/m^2)
The following is important information regarding the input terminal connector: Hirose Electric Co.Ltd / model:

DF9MA-41P-1V /for 12.1" applications/

Pin No	Symbol	Function	Obs.
1	GND	-	-
2	CK	Clock signal for sampling each data signal	-
3	GND	-	-
4	Hsync	Horiz. synchronous signal	the polarity of both signals is negative
5	Vsync	Vert. synchronous signal	same as above
6	GND	-	-
7	GND	-	-
8	GND	-	-
9	R0	RED data signal	-
10	R1	RED data signal	-
11	R2	RED data signal	-

Pin No	Symbol	Function	Obs.
12	GND		-
13	G0	GREEN data signal (LSB)	-
14	G1	GREEN data signal	-
15	G2	GREED data signal	-
16	G3	GREEN data signal	-
17	G4	GREEN data signal	-
18	G5	GREEN data signal MSB	-
19	GND	-	-
20	B0	BLUE data signal	-
21	B1	BLUE data signal	-
22	B2	BLUE data signal	-
23	B3	BLUE data signal	-
24	B4	BLUE data signal	-
25	B5	BLUE data signal	-
26	GND	-	-
27	ENAB	Signal to settle the hori-zontal display position	-
28	Vcc	+5.0V power supply	-
29	Vcc	+5.0V power supply	-
30	R/L	Horizontal display mode select signal	-
31	U/D	Vertical display mode select signal	-

Backlight driving

The backlight system is an edge-lighting type with double CCFT (Cold Chatode Fluorescent Tube). The characteristics of single lamp are shown in the following table:

Parameter	Symbol	Min.	Typ.	Max.	unit
Lamp current	I(L)	2.0	6.0	6.5	mArms
Lamp power consumption	P(L)	-	3.0	-	W
Lamp frequency	F(L)	20	35	60	kHz
Kick-off voltage	V(S)	- -	- -	950 1400	V(rms) V(rms)
Lamp life time	L(L)	-	50000	-	hour

NOTE:

* Lamp frequency may produce interference with horizontal synchronous frequency, and this may cause beat on the display. Therefore lamp frequency shall be detached as much as possible from the horizontal synchronous frequency and from the harmonics.

* The open output voltage of the inverter shall be maintained for more than 1 sec. Otherwise the lamp may not be turned on.

* Since lamps are consumables, the life time written above is referential value and is not guaranteed by SHARP or KRISTEL

VERTICAL display position:

- The vertical display position is automatically centered in the active area at each mode of VGA, (480, 400, and 350) Each mode is selected depending on the polarity of the synchrounous signals described before.

HORIZONTAL display position

The horizontal display position is determined by ENAB (enable) signal and the input data corresponding to the rising edge of ENAB signal is displayed at the left end of the active area.

HANDLING Precautions

-Be sure to turn off the power supply when inserting or disconnecting the video cable.

-Since the front polarizer is easily damaged, avoid contact with rough or sharp objects

-Wipe off water drop's immediately. Extended contact with water may cause discoloration or spots.

-When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.

-Since CMOS LSI is used in this module, use ESD protection when handling

-The panel module has circuitry PCB's on its back side and should be noted not to handle or short in any way

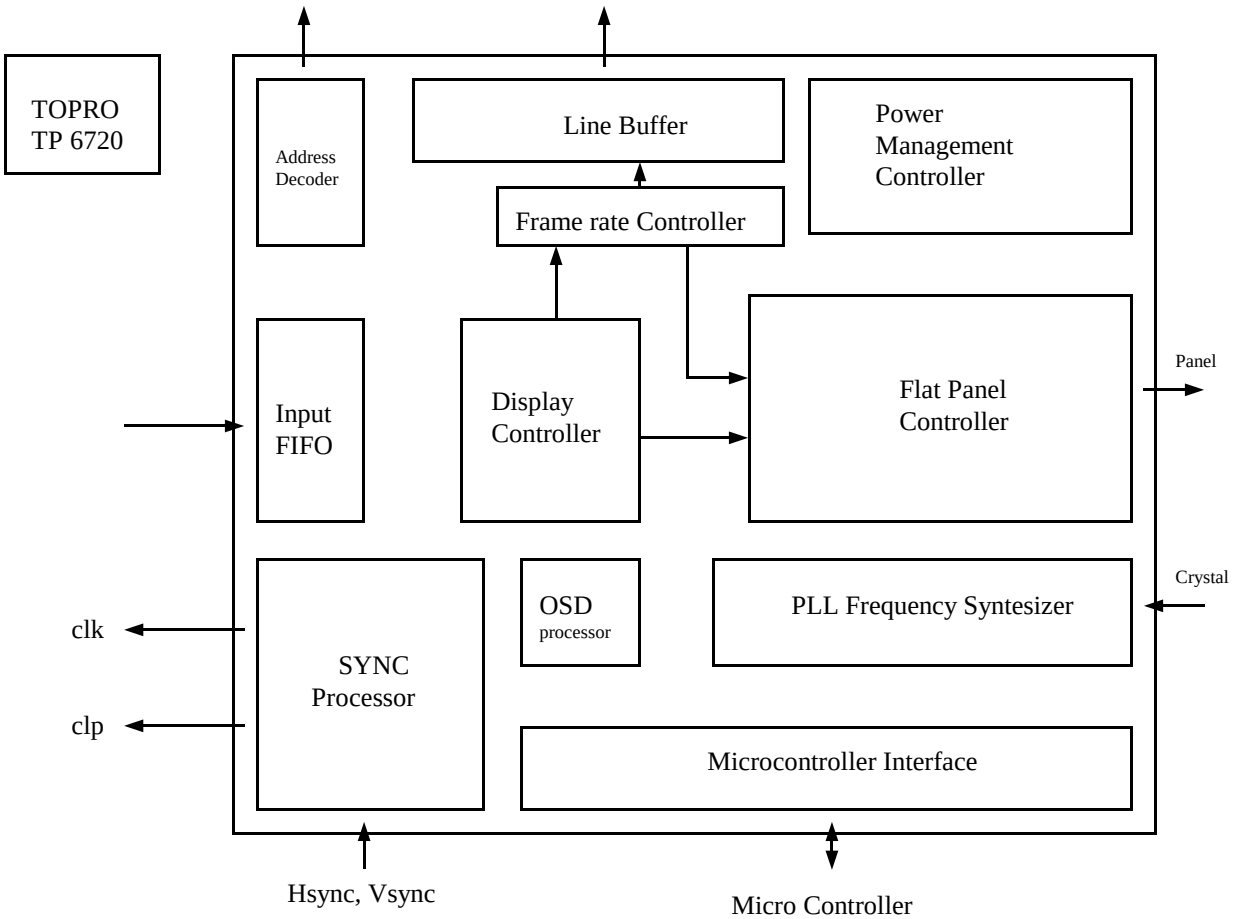
-Laminated film is attached to the module surface to prevent it from being scrached. Peel the film off slowly, just before the use, with strict attention to electrostatic charges.

-There are high voltage portions on the backlight . Careless touch may lead to electrical shock. Please send unit back to KRISTEL for authorized lamp replacement.

-Disassembling the LCD module can cause permanent damage and will void warranty.

-Please be careful since image retention may occur when a fixed pattern is displayed for a long time.

PVIP panel video / image processor, TP 6720 / TOPRO is a single chip monitor controller and contain all the logic required to convert PC VGA signals to TFT lcd signals. The chip contain 208 pins:
-Memory controller (MEMC)
-OSD Controller (OSDC)
-Display Mode Detector (DMD)
-Address Multiplexer (AMUX)
-Power Management Controller (PMC)
-Flat panel Controler
-RGB Space converetr
-24/16/12 bit digital data input selection
-VGA input Sync. capability Hsync: 15kHz ~ 60kHz, Vsync: 55 ~ 90 Hz
-Support resolution up to 1024 x 768

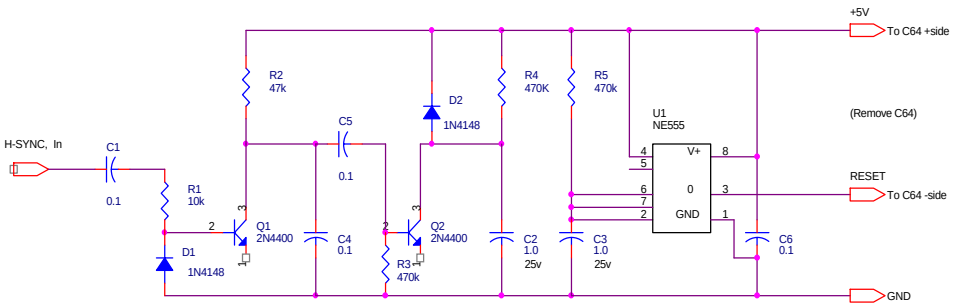


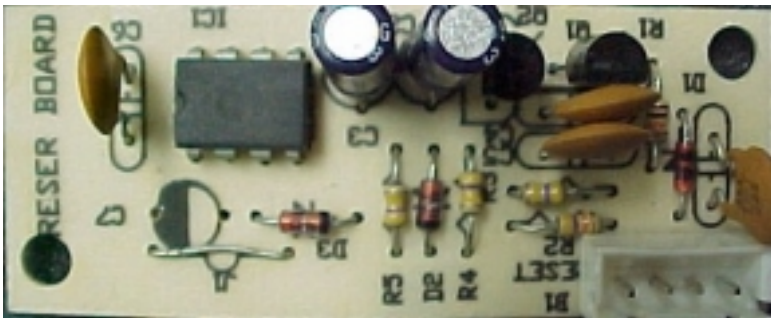
The following is a simple chart for debugging a flat panel. The symptom are listed on the left side of the column and the possible causes are on the right, with the most basic problems listed first to display specific fine tuning at the end.

SYMPTOM	POSSIBLE PROBLEM
Display is completly black	Backlight is not operating 1.backlight is not hooked up, verify that the connector is plugged in completely 2.check that backlight inverter can supply the correct voltage and current for backlight 3.backlight tube has been damaged
Backlight is on but no display	Sync. signal and Display supply voltage are not being driven correctly. Specifically check Hsync, Vsync and input voltages 1.be sure data input connector is seated correctly 2.verify that the data cable is wired correctly 3.verify the input signals are at the correct active level and are within the display's specs. Always check this signals at the input connector. 4.with display hooked up verify that contrast voltages are still with spec. 5.check power sequancing applied after mods.
Information visible but badly scrambled on display	Input signals to the display are not correct. The LCD will try to operate if the input signals are close to correct 1.check Hsync, Vertsync, and clock to be sure they are within spec limits. 2.be sure Vcc and sync signals do not have excessive noise 3.verify at the input connector that each pin has the correct signal
Information is correct, but data jitters or blurs	Clock to data setup and hold time is being violated or excessive noise on data. Cable length problem. 1..reduce cable length to as short as possible 2..reduce loading on dot clock signal

SYMPTOM	POSSIBLE PROBLEM
	3.add termination to clock line 4.use high quality cable for interconnect 5.buffer output signals
Display jumps vertically	Noise on Vsync is causing false triggers to the LCD 1.reduce cable lenghts 2.add in line resistanse to Vsync line engineering issue 3.1pF cap on Vsync to filter noise
Image tears or jumps horizontally	Noise on Hsync is causing false triggers to the LCD 1.reduce cable lenghts 2.add inline resistance to Hsync line engineering issue 3.1pF cap on Hsync to filter noise
Color are not correct	The data lines between the controller and the display are not connected correctly. 1.wirring error. Verify connections between display and controller / Hirose cable, DF9MA-41P-1V/ 2.video cable problem /sequance/
Video come up after a while	Start up circuit problem. Check the functionality / re-place start up daughter board.
Display appears to be washed out, poor contrast	Contrast voltage is not set properly 1.verify contrast is set correctly at optimum level 2.verify vertical sync timing is correct
	Reffer to “buildbook” and check all the modifications that was set for this particular model. If the problem persist, contact your supervisor for assistance.

NOTE: actual information subject to modification and improvement



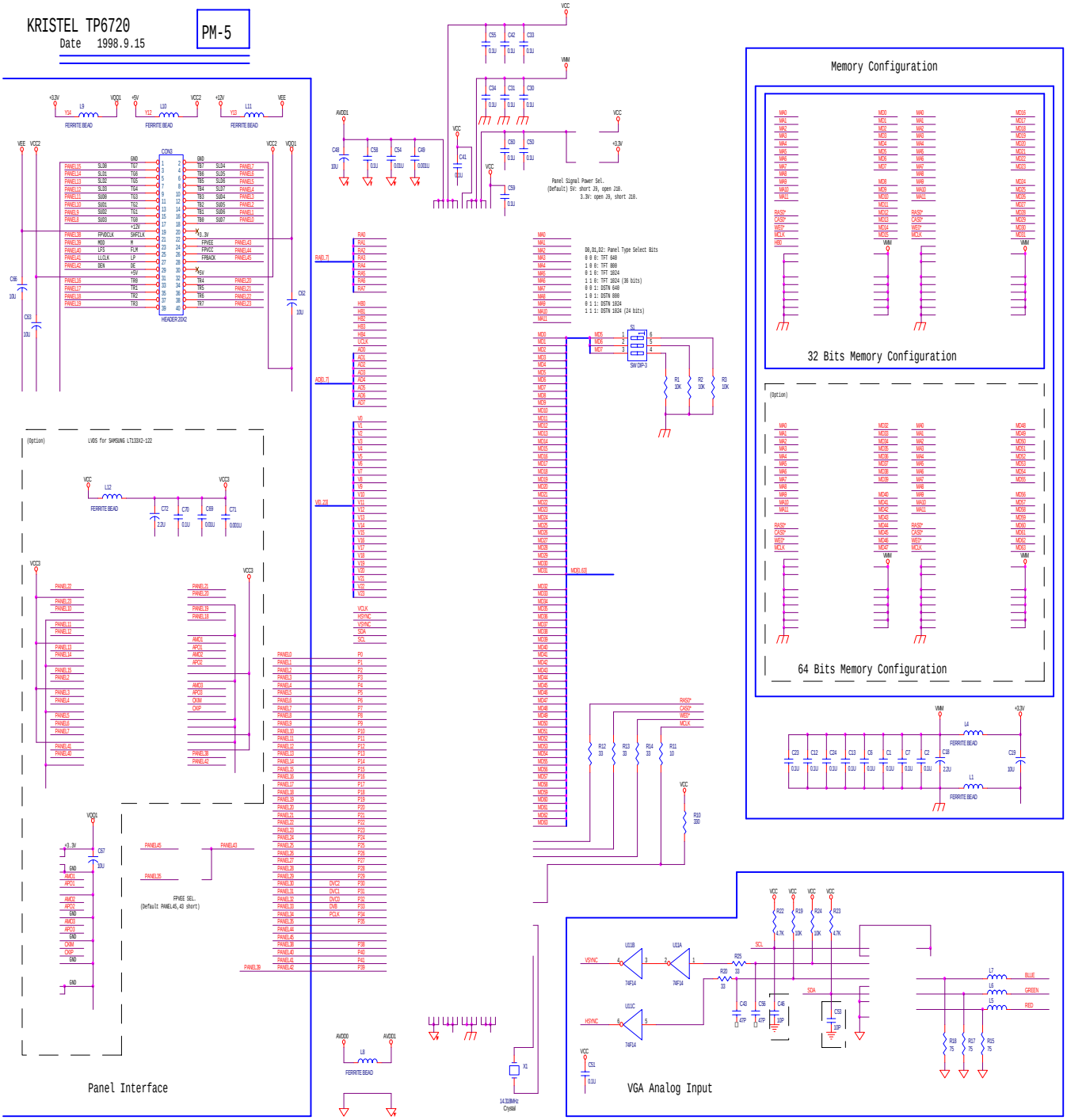


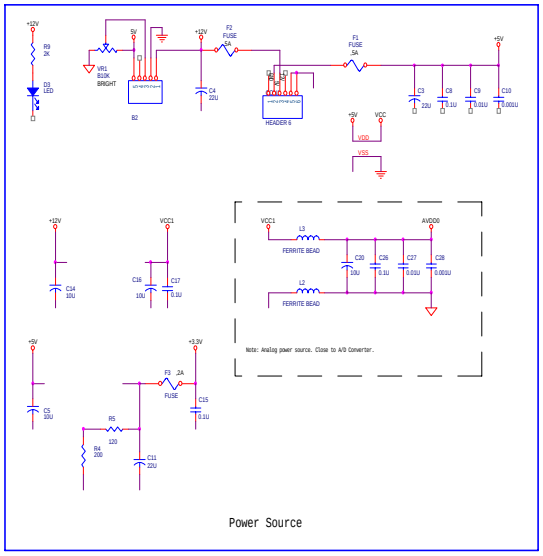
Title	KRISTEL AD-RESET1.sch		
Size A4	Document Number RESET circuit for TP6720 A/D card	drawing by: 2M	Rev <RevCode>
Date: Friday, February 25, 2000	Sheet 1 of 1		

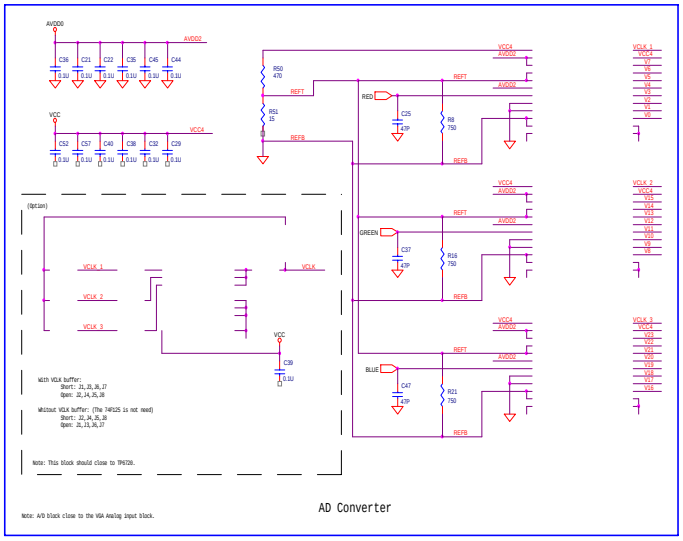
KRISTEL TP6720

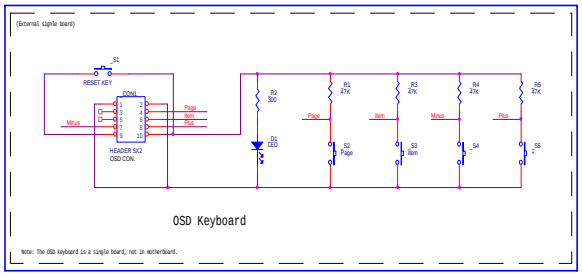
Date 1998.9.15

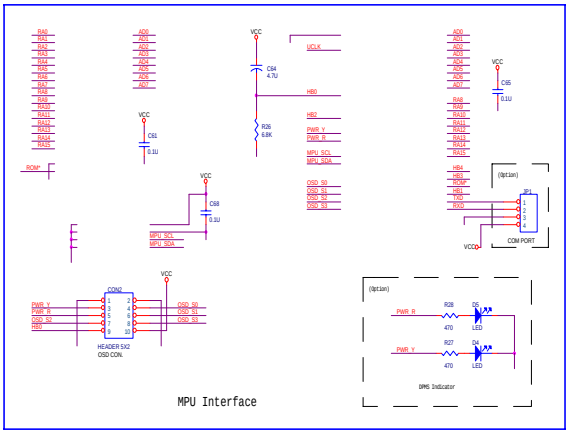
PM-5

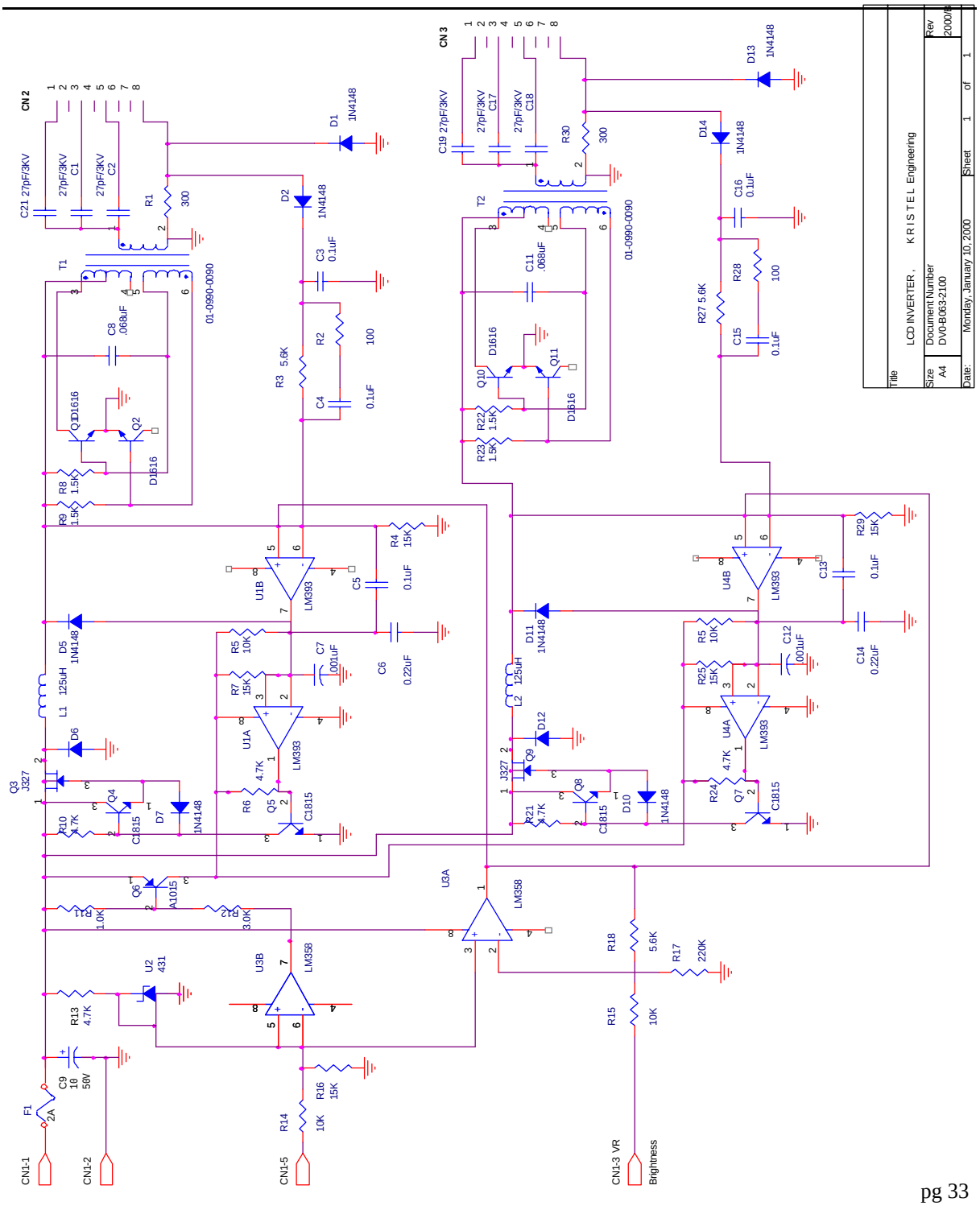



Power Source


AD Converter


OSD Keyboard


MPU Interface


CN 2
CN 3
T1
T2
01-0990-0090
C21 27pF/3KV
C1 27pF/3KV
C2 27pF/3KV
C19 27pF/3KV
C17 27pF/3KV
C18 27pF/3KV
R1 300
R30 300
D1 1N4148
D2 1N4148
D13 1N4148
D14 1N4148
C3 0.1uF
C16 0.1uF
C8 .068uF
C11 .068uF
R2 100
R28 100
R3 5.6K
R27 5.6K
C4 0.1uF
C15 0.1uF
Q1 D1616
Q2 D1616
Q10 D1616
Q11 D1616
R8 1.5K
R9 1.5K
R22 1.5K
R23 1.5K
U1B LM393
U4B LM393
R4 15K
R29 15K
C5 0.1uF
C13 0.1uF
C6 0.22uF
C14 0.22uF
D5 1N4148
D11 1N4148
L1 125uH
L2 125uH
R5 10K
R5 10K
R7 15K
R25 15K
C7 .001uF
C12 .001uF
U1A LM393
U4A LM393
D6
D12
Q3 J327
Q9 J327
Q4 C1815
Q8 C1815
Q5 C1815
Q7 C1815
D7 1N4148
D10 1N4148
R6 4.7K
R24 4.7K
R10 4.7K
R21 4.7K
Q6 A1015
R11 1.0K
R12 3.0K
U3A LM358
U2 431
U3B LM358
R13 4.7K
R18 5.6K
R17 220K
R15 10K
C9 10 50V
F1 2A
R16 15K
R14 10K
CN1-1
CN1-2
CN1-5
CN1-3 VR
Brightness
Title
LCD INVERTER , KRISTEL Engineering
Size A4
Document Number DV0-B063-2100
Rev 2000
Date: Monday, January 10, 2000
Sheet 1 of 1

TFT-LCD module, LQ121S1DG11
This module is a color active matrix LCD incorporating amorphous silicon TFT (Thin film transistor)

Overview
Graphics and texts can be displayed on a 800x600 dots panel with 262,144 colors by supplying 18 bits data signal (6bit/color), four timing signals, +3.3V/5V DC supply voltage for TFT-LCD panel driving and supply voltage for backlight.
The TFT-LCD used for this module is a low-reflection and higher-color-saturation type.

1. Mechanical Specifications

PARAMETER	SPECIFICATIONS	UNIT
Display size	31 (12.1") Diagonal	cm
Active areea	246.0(H) x 184.5(V)	mm
Pixel format	800(H)x600(V)	pixel
Pixel pitch	0.3075(H)x0.3075(V)	mm
Pixel config.	R,G,B vertical stripe	-
Display mode	Normally white	-
Mass	Customer chassis specification	-
Surface treatment (for panel)	Anti-glare and hardcoating 3H	-

2. TFT-LCD panel driving interface connector:

DF9MA-41P-1V (Hirose Electric Co) , 41 pins

3. Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITION	RATINGS	UNIT	NOTE
Input Voltage	Vi	T=25^{0}C	0.3~	V	-
Supply voltage	Vcc	Ta=25^{0}C	0~+6	V	-
Storage Temp.	Tstg	-	-25~+60	^{0}C	humid. 95%max
Operating temp.	Top	-	0~+50	^{0}C	no condensation

4. Timing characteristics

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNIT	REMARK
CLOCK	Frequency	1 / Tc	-	40.0	42.0	MHz	-
	High time	Tch	6	-	-	ns	-
	Low time	Tcl	6	-	-	ns	-
	Duty ratio	Th / T	40	50	60	%	-
DATA	Setup time	Tds	3	-	-	ns	-
	Hold time	Tdh	10	-	-	ns	-
Horizontal sync.signal	cycle	TH	20.8	26.4	-	microsec.	-
			832	1056	-	clock	-
	Pulse width	THp	2	128	200	clock	-
Vertical sync.signal	cycle	TV	628	666	798	line	-
	Pulse width	TVp	2	4	6	line	-
Horiz. displ. period		THd	800	800	800	clock	-
Hsync-clock phase diff		THc	0	-	Tc10	ns	-
Hsync Vsync phase diff.		TVh	0	-	Th-THP	ns	-
Vertical data start position		TVs	23	23	23	line	-
obs.							

5. Reliability test

No	Test item	Conditions
1.	High temperature storage test	Ta=60^{0}C 240h
2.	Low temperature storage	Ta= -25^{0}C 240h
3.	High temp. & humidity operation	Ta=40^{0}C 240h / no condens./
4.	High temp. operation test	Ta=50^{0}C 240h
5.	Low temperature operation test	Ta=0^{0}C 240h
6.	Vibration test none	Frequency: 10 ~57 Hz / Vibration width (one side) 58~500Hz /Gravity: 9.8m/s^2
7.	Shock test (non-operating)	Max. gravity: 490 m/s^2, direction +/-X,+/-Y,+/-Z once for each dir.

Under the display quality test conditions with normal operation state, these shall have no change which may affect practical display function

NOTE:

1. Disassembling the module can cause permanent damage and should be strictly avoided

2. Please be careful since image retention may occur when a fixed pattern is displayed for a long time.

3. If any problem occurs in relation to the description of this specification, it shall be resolved through discussion with spirit of cooperation

KRISTEL Engineering
2_M

01 / 2000